19-3974; Rev 0; 1/06

EVALUATION KIT AVAILABLE

High-Speed, Dual-Phase Driver with Integrated Boost Diodes

General Description

The MAX8811 2-phase gate driver controls power MOSFETs in multiphase synchronous step-down converter applications, providing up to 30A output current per phase. The MAX8811 and MAX8810A (multiphase power-supply controller) combine to provide an efficient, low-cost solution for a wide range of multiphase power-supply applications. The MAX8811 handles system input voltages up to 26V. Each MOSFET driver is capable of driving 3000pF capacitive loads with 11ns typical rise and fall times.

Adaptive shoot-through protection circuitry is implemented to prevent shoot-through currents for the "high-side off to low-side on" transition. A programmable delay is provided for the "low-side off to high-side on" transition. This maximizes overall converter efficiency while supporting operation with a variety of MOSFETs.

The MAX8811 provides an easy upgrade path from the MAX8523 dual driver. Integrated bootstrap diodes reduce external component count, while an enable input provides flexibility for power sequencing. The MAX8811 is available in a space-saving, 16-pin QSOP.

Applications

Processor Core Voltage Regulators

Multiphase Buck Converters

Voltage-Regulator Modules (VRMs)

Switching Power Supplies

DC-DC Converter Modules

Features

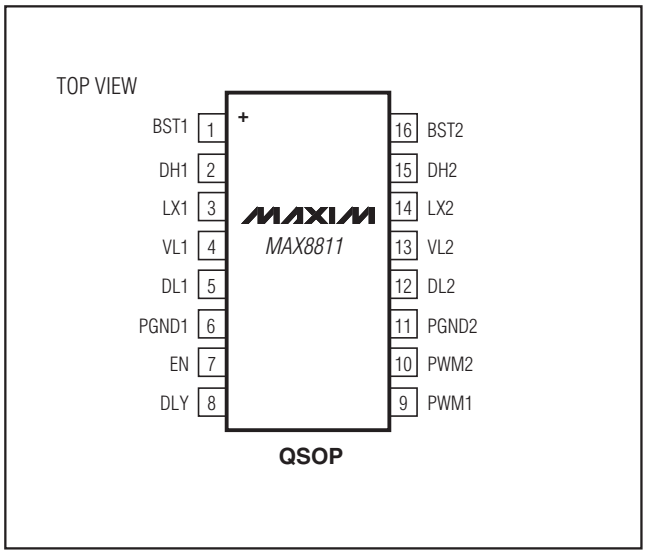
- **Dual-Phase Synchronous Buck Driver**
- **Integrated Bootstrap Diodes**
- **Up to 26V System Input Voltage**
- **6A Peak Gate Drive Current**
- **Capable of 30A per Phase**
- **0.4Ω/0.9Ω Low-Side, 0.7Ω/1.0Ω High-Side Drivers (typ)**
- **Typical 11ns Rise/Fall Times with 3000pF Load**
- **Adaptive Dead-Time Control**
- **User-Programmable Delay Time**
- **Enable Function with 0.04µA (typ) Quiescent Current in Shutdown**
- **Space-Saving, Lead-Free, 16-Pin QSOP**

Ordering Information

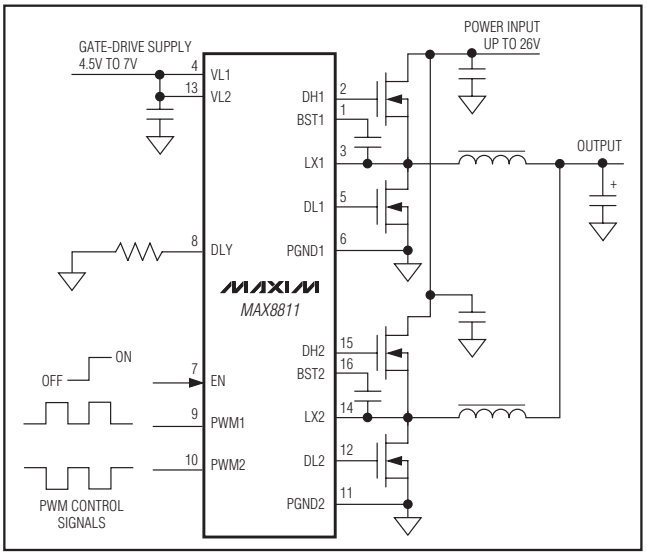
PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX8811EEE+	-40°C to +85°C	16 QSOP	E16-4

+ = Denotes lead-free package.

Pin Configuration



Typical Operating Circuit



High-Speed, Dual-Phase Driver with Integrated Boost Diodes

ABSOLUTE MAXIMUM RATINGS

DLY, EN to PGND_, PWM_ to DL_.....-0.3V to ($V_{VL\_}$ + 0.3V)
BST_ to PGND_ .....-0.3V to ($V_{LX\_}$ + 8V)
BST_ to VL_ .....-1V to +30V
LX_ to PGND_.....-1V to +28V
DH_ to PGND_.....-0.3V to ($V_{BST\_}$ + 0.3V)
DH_, BST_ to LX_ .....-0.3V to +8V
VL_ to PGND_ .....-0.3V to +8V
DH_, DL_ Current ..... ±200mA RMS
VL_ to BST_ Internal Diode Current .....±50mA RMS
PGND1 to PGND2 .....-0.3V to +0.3V
Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 8.3 mW/°C above +70°C).....666.7 mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DLY} = V_{EN} = $V_{BST\_}$ = $V_{VL\_}$ = 6.5V, $V_{PGND\_}$ = $V_{LX\_}$ = $V_{PWM\_}$ = 0V, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL					
VL_ Input Voltage Range		4.5		7	V
LX Operating Range				26	V
VL_ Undervoltage Lockout (UVLO)	$V_{VL\_}$ rising, 250mV hysteresis (typ)	3.25		3.8	V
Supply Current (per Channel) $I_{BST\_}$ + $I_{VL\_}$	$V_{PWM\_\_}$ = 0V		0.7	1.5	mA
	$V_{PWM\_\_}$ = V_{DLY} = $V_{VL\_}$		1.4	2	
Shutdown Supply Current (per Channel) $I_{BST\_}$ + $I_{VL\_}$	V_{EN} = 0V, $V_{PWM\_}$ = 0V or $V_{VL\_}$		0.04	1	µA
PWM_					
Input Leakage	$V_{PWM\_}$ = 0V or 7.0V, V_{EN} = 0V or 7.0V		0.01		µA
Input Voltage High Threshold					V
Input Voltage Low Threshold		1.2		3.5	V
Input Threshold Hysteresis			20		%
EN					
Input Leakage	$V_{PWM\_}$ = 0V or 7.0V, V_{EN} = 0V or 7.0V		0.01		µA
Input Voltage High Threshold		0.8			V
Input Voltage Low Threshold				2.6	V
Input Voltage Hysteresis			0.5		V
DLY					
Delay Disable Threshold $V_{VL\_}$ - V_{DLY}			0.8	1.2	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DLY} = V_{EN} = $V_{BST\_}$ = $V_{VL\_}$ = 6.5V, $V_{PGND\_}$ = $V_{LX\_}$ = $V_{PWM\_}$ = 0V, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GATE DRIVER SPECIFICATIONS						
DH_ Driver Resistance	$V_{PWM\_}$ = $V_{VL\_}$, sourcing current	$V_{BST\_}$ = 6.5V, $I_{DH\_}$ = -0.1A		1.0	1.6	Ω
	$V_{PWM\_}$ = 0V, sinking current	$V_{BST\_}$ = 6.5V, $I_{DH\_}$ = 0.1A		0.7	1.1	
DL_ Driver Resistance	$V_{PWM\_}$ = 0V, sourcing current	$V_{VL\_}$ = 6.5V, $I_{DL\_}$= -0.1A		0.9	1.5	
	$V_{PWM\_}$ = $V_{VL\_}$, sinking current	$V_{VL\_}$= 6.5V, $I_{DL\_}$= 0.1A		0.4	0.7	
DH_ Rise Time (t_{rDH})	$V_{PWM\_}$ = $V_{VL\_}$	$V_{BST\_}$ = 6.5V, 3000pF load		14		ns
DH_ Fall Time (t_{fDH})	$V_{PWM\_}$ = 0V	$V_{BST\_}$ = 6.5V, 3000pF load		9		ns
DL_ Rise Time (t_{rDL})	$V_{PWM\_}$ = 0V	$V_{VL\_}$ = 6.5V, 3000pF load		11		ns
DL_ Fall Time (t_{fDL})	$V_{PWM\_}$ = $V_{VL\_}$	$V_{VL\_}$ = 6.5V, 3000pF load		8		ns
DH_ Propagation Delay	$V_{PWM\_}$ falling (t_{pDHf})	$V_{BST\_}$ = 6.5V		20		ns
	$V_{PWM\_}$ = $V_{VL\_}$, $V_{DL\_}$ falling (t_{pDHr})			14		
DL_ Propagation Delay	$V_{PWM\_}$ rising (t_{pDLf})	$V_{BST\_}$ - $V_{LX\_}$ = 6.5V		12		ns
	$V_{PWM\_}$ = GND, LX falling (t_{pDLr})			16		
INTERNAL BOOST DIODE SPECIFICATIONS						
On-Resistance	$I_{BST\_}$ = 40mA			6		Ω
THERMAL SHUTDOWN						
Thermal Shutdown	Rising temperature, hysteresis = 15°C (typ)			+165		°C

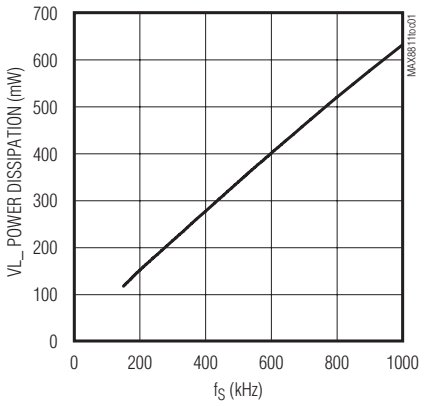
Note 1: Specifications at -40°C guaranteed by design.

High-Speed, Dual-Phase Driver with Integrated Boost Diodes

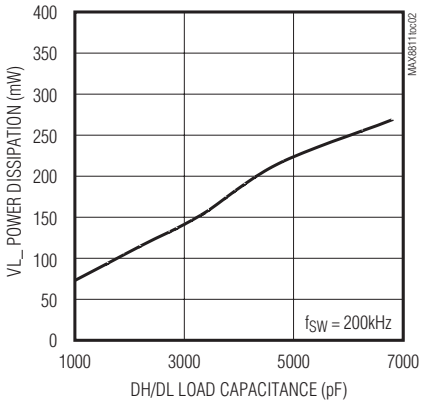
Typical Operating Characteristics

(V_{VL1} = V_{VL2} = V_{EN} = V_{DLY} = 6.5V, 3000pF capacitive load, T_A = +25°C, unless otherwise noted.)

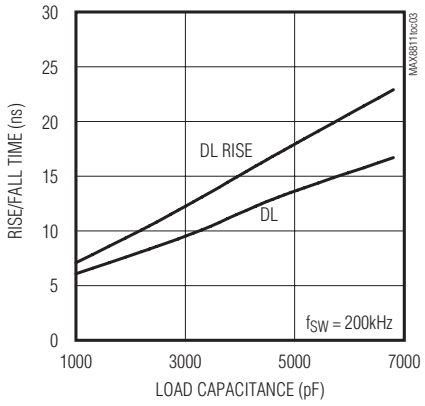
VL_ POWER DISSIPATION vs. PER-PHASE SWITCHING FREQUENCY



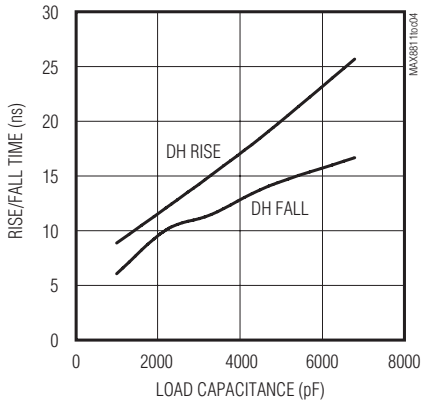
VL_ POWER DISSIPATION vs. LOAD CAPACITANCE



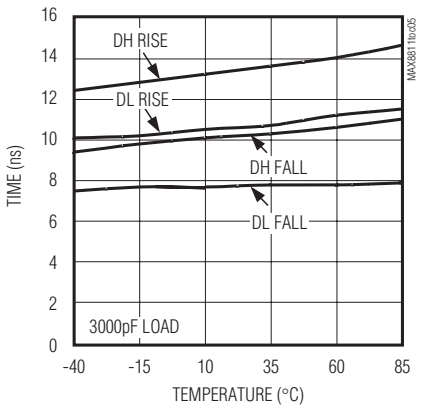
DL RISE/FALL vs. LOAD CAPACITANCE



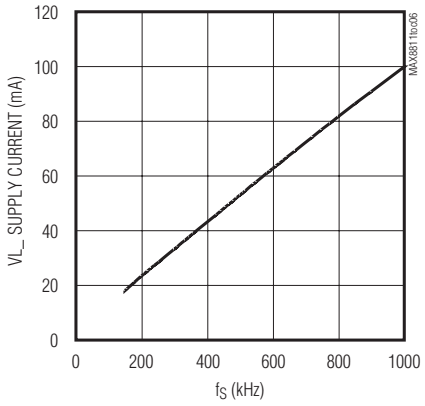
DH RISE/FALL TIME vs. LOAD CAPACITANCE



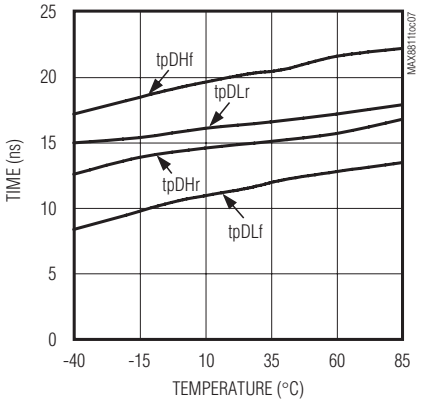
RISE AND FALL TIMES vs. TEMPERTURE



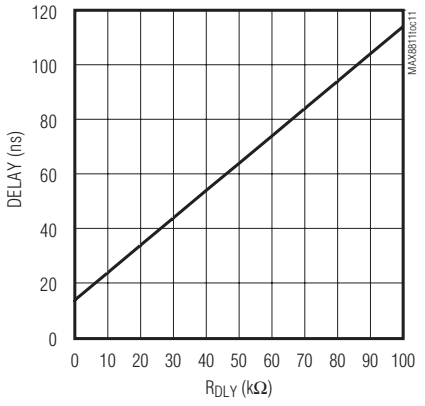
VL_ SUPPLY CURRENT vs. PER-PHASE SWITCHING FREQUENCY



PROPAGATION DELAY vs. TEMPERATURE



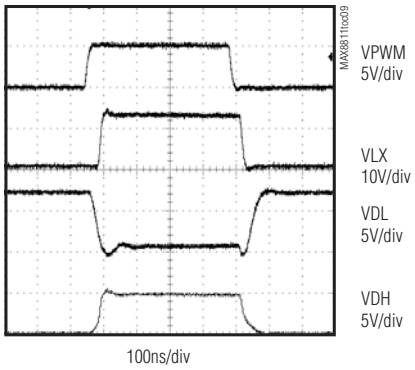
PROGRAMMABLE DELAY vs. R_{DLY}



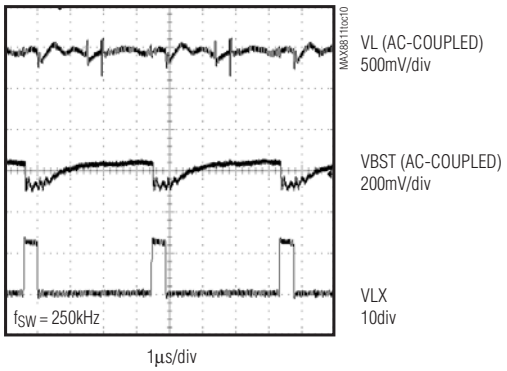
Typical Operating Characteristics (continued)

(V_{VL1} = V_{VL2} = V_{EN} = V_{DLY} = 6.5V, 3000pF capacitive load, T_A = +25°C, unless otherwise noted.)

SWITCHING WAVEFORMS



VBST_ AND VL_ WAVEFORMS



Pin Description

PIN	NAME	FUNCTION
1	BST1	Boost Capacitor Connection for Phase 1. Connect a 0.22µF ceramic capacitor between BST1 and LX1.
2	DH1	High-Side Gate-Driver Output for Phase 1. DH1 is pulled low during shutdown and UVLO.
3	LX1	Inductor Connection for Phase 1
4	VL1	Gate-Drive Supply for DL1. Connect VL1 to a 4.5V to 7V supply. VL1 must be connected to VL2 externally. Bypass the VL1/VL2 connection with a 2.2µF or larger ceramic capacitor to the power ground plane.
5	DL1	Low-Side Gate-Driver Output for Phase 1. DL1 is pulled low during shutdown and UVLO.
6	PGND1	Power Ground for DL1. Connect PGND1 and PGND2 to the power ground plane at the IC.
7	EN	Enable Input. Drive EN high for normal operation, or low for shutdown.
8	DLY	Delay Time Setting Input. Connect a resistor from DLY to PGND1 to set the dead time between DL falling and DH rising, or connect DLY to VL1 to use the default delay.
9	PWM1	PWM Logic Input for Phase 1. DH1 is high when PWM1 is high; DL1 is high when PWM1 is low.
10	PWM2	PWM Logic Input for Phase 2. DH2 is high when PWM2 is high; DL2 is high when PWM2 is low.
11	PGND2	Power Ground for DL2. Connect PGND1 and PGND2 to the power ground plane at the IC.
12	DL2	Low-Side Gate-Driver Output for Phase 2. DL2 is pulled low during shutdown and UVLO.
13	VL2	Gate-Drive Supply for DL2. Connect VL2 to a 4.5V to 7V supply. VL1 must be connected to VL2 externally. Bypass the VL1/VL2 connection with a 2.2µF or larger ceramic capacitor to the power ground plane.
14	LX2	Inductor Connection for Phase 2
15	DH2	High-Side Gate-Driver Output for Phase 2. DH2 is pulled low during shutdown and UVLO.
16	BST2	Boost Capacitor Connection for Phase 2. Connect a 0.22µF ceramic capacitor between BST2 and LX2.

High-Speed, Dual-Phase Driver with Integrated Boost Diodes

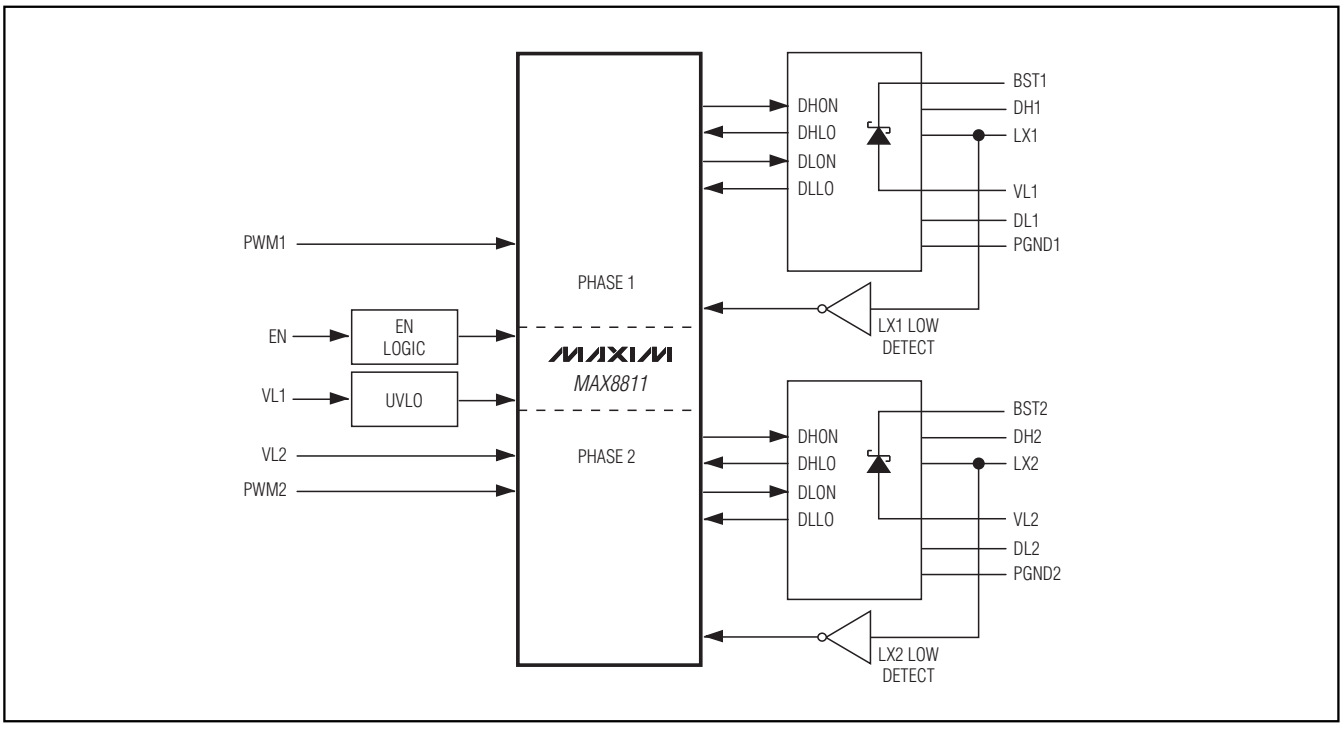


Figure 1. Functional Diagram

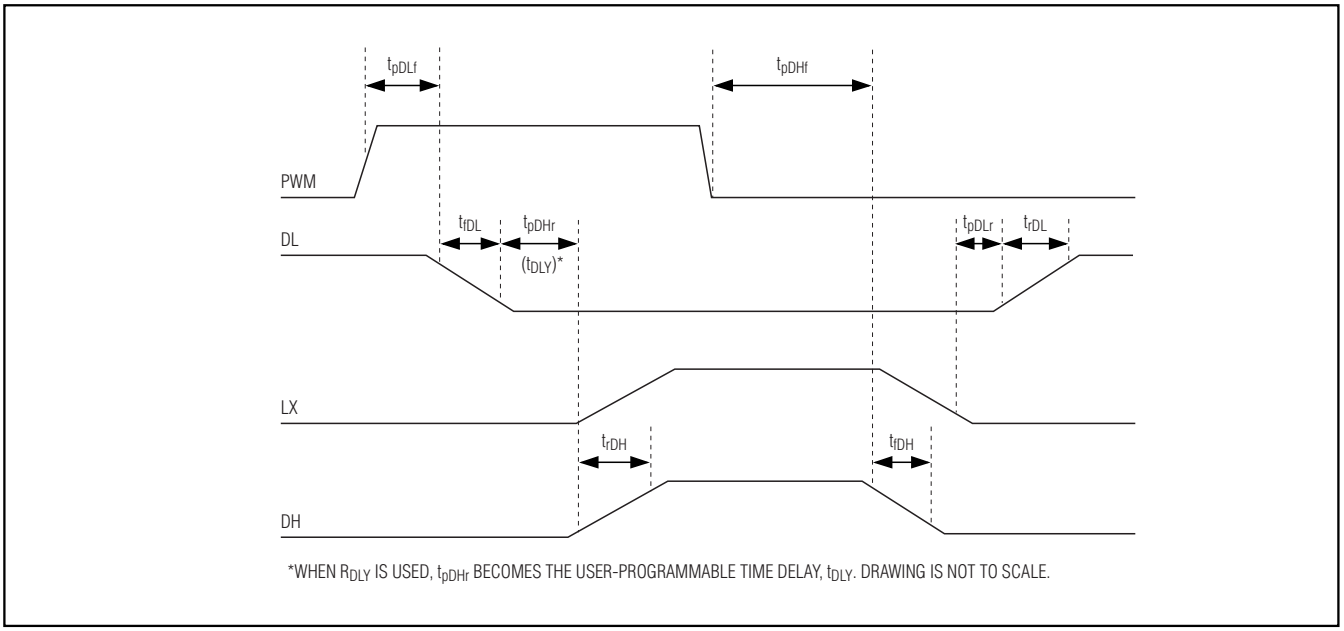


Figure 2. Driver Timing Diagram

Detailed Description

Principles of Operation

MOSFET Gate Drivers (DH_, DL_)

DH_ is driven high when the PWM_ is high; DL_ is driven high when PWM_ is low. PWM pulsewidths under 20ns (typ) are rejected, and no switching occurs.

The low-side drivers (DL_) have typical 0.9µs sourcing resistance and 0.4Ω sinking resistance, and are capable of driving 3000pF capacitive loads with 11µs typical rise and 8µs typical fall times. The high-side drivers (DH_) have typical 1.0Ω sourcing resistance and 0.7Ω sinking resistance, and are capable of driving 3000pF capacitive loads with 14µs typical rise and 9µs typical fall times. This facilitates fast switching, reducing switching losses, and makes the MAX8811 ideal for both high-frequency and high-output current applications.

Shoot-Through Protection

Adaptive shoot-through protection is incorporated for the switching transition after the high-side MOSFET is turned off and before the low-side MOSFET is turned on. The low-side driver is turned on when the LX voltage falls below 2.5V, or after 135ns typical delay, whichever occurs first. Furthermore, the delay time between the low-side MOSFET turn-off and high-side MOSFET turn-on can be adjusted by selecting the value of R1 (see the *Setting the Dead Time* section).

Undervoltage Lockout (UVLO)

When the voltage at the VL1/VL2 connection is below the UVLO threshold, all driver outputs are held low. This prevents switching when the supply voltage is too low for proper operation.

Thermal Protection

Thermal-overload protection limits total power dissipation in the MAX8811. When the junction temperature exceeds +165°C, all driver outputs are held low. The IC resumes normal operation after the junction temperature cools by 15°C (typ).

Boost Capacitor Selection

The MAX8811 uses a bootstrap circuit to generate the supply voltages for the high-side drivers (DH_). The selected high-side MOSFET determines the appropriate boost capacitance values, according to the following equation:

$$C_{BST} = \frac{Q_{GATE}}{\Delta V_{BST}}$$

Table 1. Components for Figure 3, 800kHz, 20A/Phase Typical Application Circuit

DESIGNATION	DESCRIPTION	MANUFACTURER
C1	2 x 10µF ±20%, X7R 25V capacitor 12103D106MAT2W	AVX
C2	2 x 10µF ±20%, X7R 25V capacitor 12103D106MAT2W	AVX
C3	2.2µF ±20%, 10V X5R capacitor GRM39X5R225K10	Murata
C4, C5	0.22µF ±20%, 10V X7R capacitors GRM39X7R224K10	Murata
C6–C9	100µF ±20%, 6.3V X5R capacitors C3225X5R0J107M	TDK
L1, L2	0.2µH, 28A inductors FDV0630-R20M,1.9mΩ DCR	TOKO
Q1, Q3	HAT2168, 8mΩ, 30V MOSFET	Renesas
Q2	2 x HAT2164H, 3mΩ, 30V, MOSFET	Renesas
Q4	2 x HAT2164H, 3mΩ, 30V MOSFET	Renesas
R1	Dead-time delay programming resistor; see TOC **TBD**	—

where Q_{GATE} is the total gate charge of the high-side MOSFET and ΔV_{BST} is the voltage variation allowed on the high-side MOSFET drive. Choose ΔV_{BST} = 0.1V to 0.2V when determining C_{BST}. Low-ESR ceramic capacitors should be used.

VL_ Decoupling

VL1 and VL2 provide the supply voltage for the low-side drivers. The decoupling capacitors at VL_ also charge the BST capacitors during the time period when DL_ is high. Therefore, the decoupling capacitor C3 for VL_ should be large enough to minimize the ripple voltage during switching transitions. Choose the VL capacitor approximately 10 times the value of the BST capacitor value.

High-Speed, Dual-Phase Driver with Integrated Boost Diodes

Table 2. Components for Figure 4, 300kHz, 30A/Phase Typical Application Circuit

DESIGNATION	DESCRIPTION	MANUFACTURER
C1	2 x 10µF ±20%, X7R 25V capacitor 12103D106MAT2W	AVX
C2	2 x 10µF ±20%, X7R 25V capacitor 12103D106MAT2W	AVX
C3	2.2µF ±20%, 10V X5R capacitor GRM39X5R225K10	Murata
C4, C5	0.22µF ±20%, 10V X7R capacitors GRM39X7R224K10	Murata
C6, C7, C8	2700µF ±20%, 6.3V capacitors MFZ series, 7mΩ max ESR	Rubycon
L1, L2	T50183, 250nH inductors at 35A ±20%, 0.68mΩ DCR	Falco Electronics
Q1	2 x HAT2168, 8mΩ, 30V MOSFET	Renesas
Q2	2 x HAT2164H, 3mΩ, 30V MOSFET	Renesas
Q3	2 x HAT2168, 8mΩ, 30V MOSFET	Renesas
Q4	2 x HAT2164H, 3mΩ, 30V MOSFET	Renesas

Setting the Dead Time

Connect DLY to VL_ for the default delay time, typically 14ns. To increase the delay between the low-side MOSFET drive turn-off and the high-side MOSFET turn-on, connect a resistor from DLY to PGND1. See the *Typical Operating Characteristics* section for a plot of the delay time vs. resistor value. The equation for this resistor is:

$$t_{DLY} = 14\mu s + (1pF) \times R_{DLY}$$

Avoiding dV/dt-Induced Low-Side MOSFET Turn-On

At high input voltages, fast turn-on of the high-side MOSFET could momentarily turn on the low-side MOSFET due to the high dV/dt appearing at the drain of the low-side MOSFET. The high dV/dt causes a current flow through the Miller capacitance (C_{RSS}) and the input capacitance (C_{ISS}) of the low-side MOSFET. Improper selection of the low-side MOSFET that has a high ratio of C_{RSS}/C_{ISS} makes the problem more severe. To avoid the problem, give special attention to the ratio of C_{RSS}/C_{ISS} when selecting the low-side MOSFET. Adding a resistor between BST_ and the BST_ capacitor slows the high-side MOSFET turn-on. Adding a capacitor from the gate to the source of the high-side MOSFET has the same effect. However, both methods are at the expense of increasing the switching losses.

Applications Information

Power Dissipation

Power dissipation in the IC package comes mainly from switching the MOSFETs. Therefore, it is a function of both switching frequency and the total gate charge of the selected MOSFETs. The total power dissipation when both drivers are switching is given by:

$$P_{IC} = 2 \times f_S \times [N \times Q_{G\_TOTAL\_HS} \times \frac{R_{HS}}{R_{HS} + (R_{G\_HS} / N)} + M \times Q_{G\_TOTAL\_LS} \times \frac{R_{LS}}{R_{LS} + (R_{G\_LS} / M)}] \times V_{PV\_} + V_{VCC} \times I_{VCC}$$

where f_S is the switching frequency, $Q_{G\_TOTAL\_HS}$ is the total gate charge of the selected high-side MOSFET, $Q_{G\_TOTAL\_LS}$ is the total gate charge of the selected low-side MOSFET, N is the total number of the high-side MOSFETs in parallel, M is the total number of the low-side MOSFETs in parallel, V_{VL} is the voltage at VL, R_{HS} is the on-resistance of the high-side MOSFET, and R_{G_LS} is the gate resistance of the selected low-side MOSFETs.

PC Board Layout

The MAX8811 sources and sinks large currents to drive MOSFETs at high switching speeds. The high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following PC board layout guidelines are recommended when designing with the MAX8811:

1) Place all decoupling capacitors as close to their respective pins as possible.
2) Minimize the high-current loops from the input capacitor, upper switching MOSFET, and low-side MOSFET back to the input capacitor negative terminal.
3) Provide enough copper area at and around the

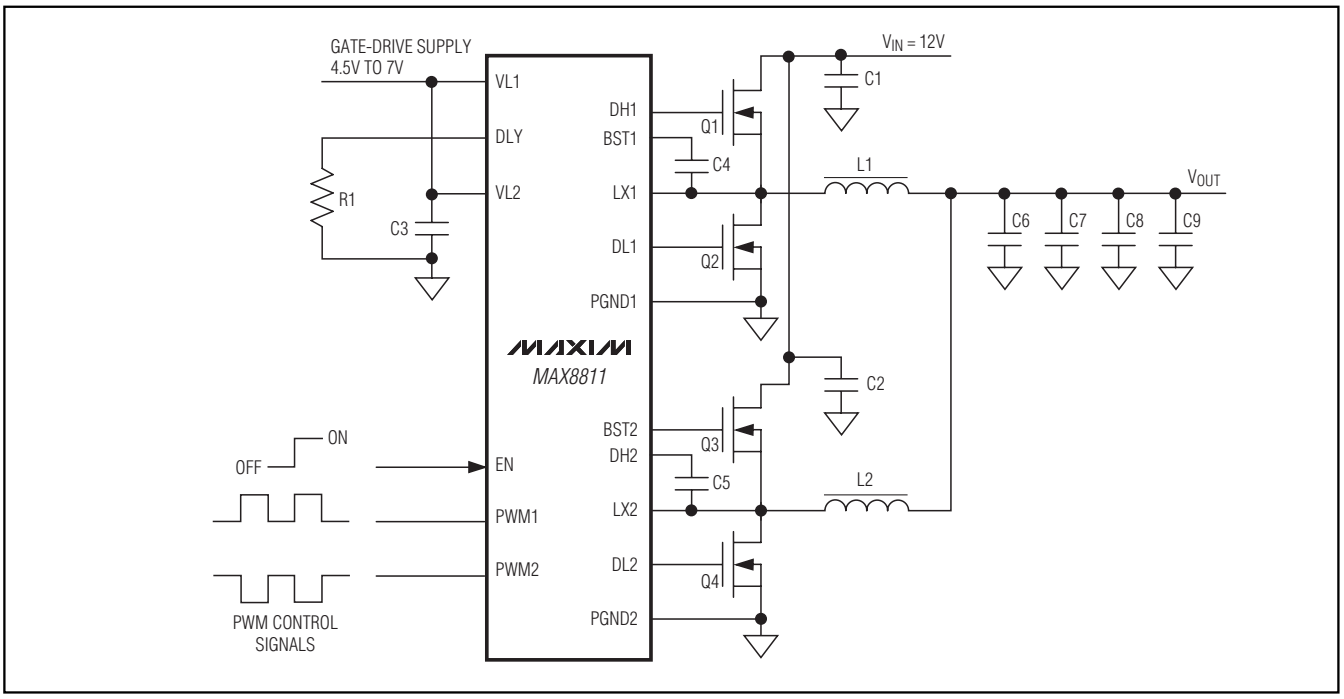


Figure 3. 800kHz, 20A/Phase Typical Application Circuit

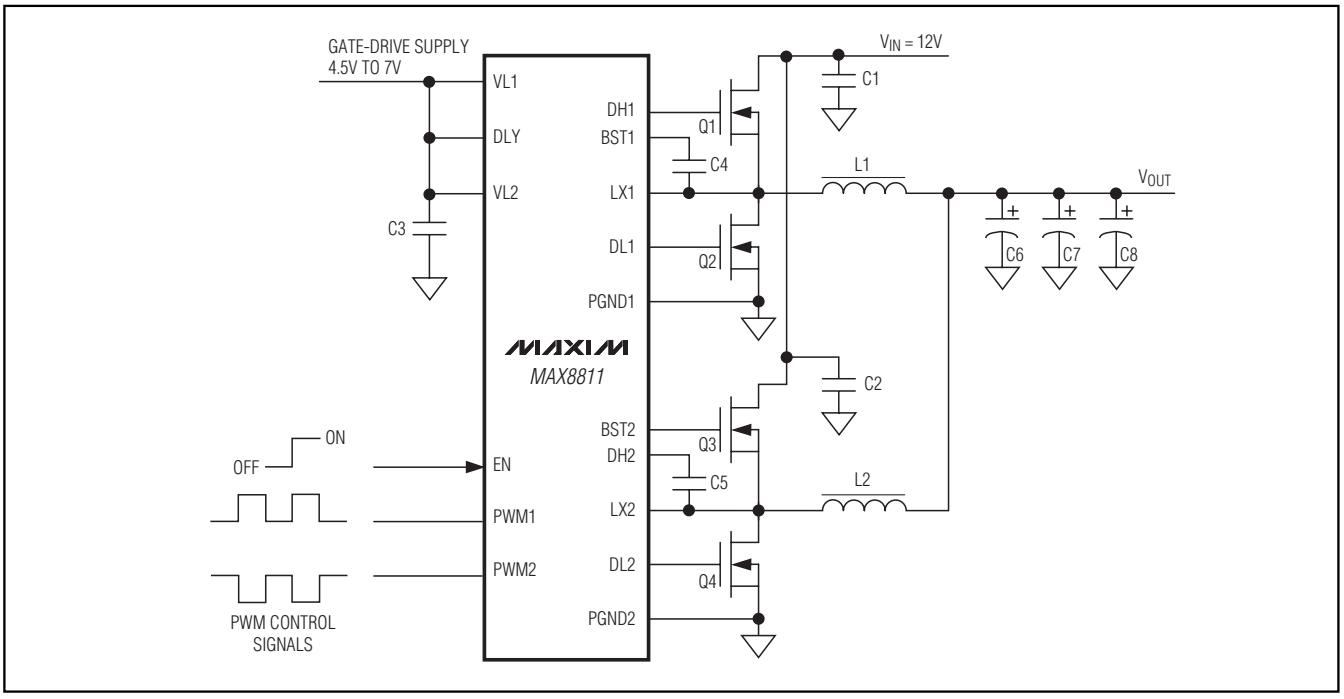


Figure 4. 300kHz, 30A/Phase Typical Application Circuit

switching MOSFETs and inductors to aid in thermal dissipation.

4) Connect PGND1 and PGND2 as close as possible to the source of the low-side MOSFETs.
5) Keep LX1 and LX2 away from sensitive analog components and nodes.
6) Gate drive traces should be at least 20 mils wide, kept as short as possible, and tightly coupled to reduce EMI and ringing induced by high-frequency gate noise. Adjacent DH_ and LX_ traces should be tightly coupled.

A sample evaluation layout is available in the MAX8811 Evaluation Kit.

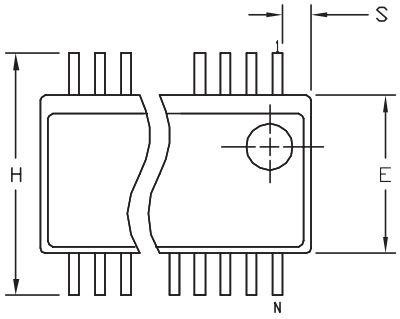
Chip Information

PROCESS: BiCMOS

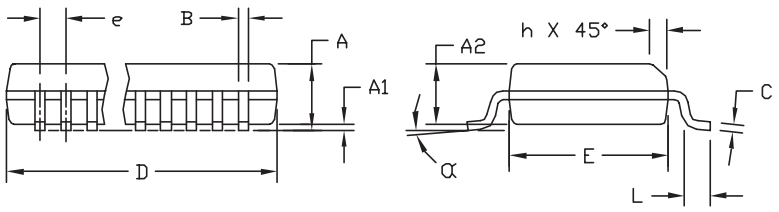
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QSOP.EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.053	.069	1.35	1.75
A1	.004	.010	.102	.254
A2	.049	.065	1.245	1.651
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°



VARIATIONS:

	INCHES		MILLIMETERS			
	MIN.	MAX.	MIN.	MAX.	N	
D	.189	.196	4.80	4.98	16	AB
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AD
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AE
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AF
S	.0250	.0300	0.635	0.762		

NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0055	F	1/1